Certification Report

Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1

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Certificate

Standard	Common Criteria for Information Technology Security Evaluation (CC), Version 3.1 Revision 4 (ISO/IEC 15408)
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TÜV Rheinland Nederland B.V. certifies:

Certificate holder and developer	**NXP Semiconductors Germany GmbH, Business Unit Security and Connectivity** **Stresemannallee 101, D-22529 Hamburg, Germany**
Product and assurance level	**Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1** Assurance Package: ▪ EAL6 augmented with ALC_FLR.1 and ASE_TSS.2 Protection Profile Conformance: ▪ Security IC Platform Protection Profile, Version 1.0, 15.06.2007; Registered and Certified by Bundesamt für Sicherheit in der Informationstechnik (BSI) under the reference BSI-PP-0035
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Common Criteria Recognition Arrangement for components up to EAL4

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Foreword

The Netherlands Scheme for Certification in the Area of IT Security (NSCIB) provides a third-party evaluation and certification service for determining the trustworthiness of Information Technology (IT) security products. Under this NSCIB, TÜV Rheinland Nederland B.V. has the task of issuing certificates for IT security products as well as for protection profiles and sites.

Part of the procedure is the technical examination (evaluation) of the product, protection profile or site according to the Common Criteria assessment guidelines published by the NSCIB. Evaluations are performed by an IT Security Evaluation Facility (ITSEF) under the oversight of the NSCIB Certification Body, which is operated by TÜV Rheinland Nederland B.V. in cooperation with the Ministry of the Interior and Kingdom Relations.

An ITSEF in the Netherlands is a commercial facility that has been licensed by TÜV Rheinland Nederland B.V. to perform Common Criteria evaluations; a significant requirement for such a license is accreditation to the requirements of ISO Standard 17025, General requirements for the accreditation of calibration and testing laboratories.

By awarding a Common Criteria certificate, TÜV Rheinland Nederland B.V. asserts that the product or site complies with the security requirements specified in the associated (site) security target, or that the protection profile (PP) complies with the requirements for PP evaluation specified in the Common Criteria for Information Security Evaluation. A (site) security target is a requirements specification document that defines the scope of the evaluation activities.

The consumer should review the security target or protection profile, in addition to this certification report, in order to gain an understanding of any assumptions made during the evaluation, the intended environment, its security requirements, and the level of confidence (i.e., the evaluation assurance level) that the product or site satisfies the security requirements stated in the (site) security target.

Recognition of the certificate

Currently the Common Criteria Recognition Arrangement (CCRA) and SOGIS-Mutual Recognition Agreement (SOGIS-MRA) do not cover the recognition of Site Certificates. However, the evaluation process followed all the rules of these agreements and used the agreed supporting document for Site certification *[CCDB]*. Therefore, the results of this evaluation and certification procedure can be re-used by any scheme in a subsequent product evaluation and certification procedure that makes use of certified site.

Presence of the Common Criteria Recognition Arrangement and SOG-IS logos on the certificate would indicate that this certificate is issued in accordance with the provisions of the CCRA and the SOG-IS agreement and will be recognised by the participating nations.

International recognition

The CCRA has been signed by the Netherlands in May 2000 and provides mutual recognition of certificates based on the CC. Starting 8 September 2014 the CCRA has been updated to provide mutual recognition of certificates based on cPPs (exact use) or STs with evaluation assurance components up to and including EAL2+ALC_FLR. The current list of signatory nations and approved certification schemes can be found on: http://www.commoncriteriaportal.org.

Certificates issued before 08 September 2014 are still under recognition according to the rules of the previous CCRA (i.e. recognition based on assurance components up to and including EAL4+ALC_FLR). Also certification procedures started before 8 September 2014 and Assurance Continuity (maintenance and re-certification) of old certificates remain recognised according to the rules of the previous CCRA.

The certification of this product has started before 8 September 2014 and thus the recognition of the certificate falls under the recognition rules of the previous CCRA.

European recognition

The European SOGIS-Mutual Recognition Agreement (SOGIS-MRA) version 3 effective from April 2010 provides mutual recognition of Common Criteria and ITSEC certificates at a basic evaluation level for all products. A higher recognition level for evaluation levels beyond EAL4 (resp. E3-basic) is provided for products related to specific technical domains. This agreement was initially signed by Finland, France, Germany, The Netherlands, Norway, Spain, Sweden and the United Kingdom. Italy joined the SOGIS-MRA in December 2010. The current list of signatory nations, approved certification schemes and the list of technical domains for which the higher recognition applies can be found on: http://www.sogisportal.eu.

1 Executive Summary

This Certification Report states the outcome of the Common Criteria security evaluation of the Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1. The developer of the Crypto Library is NXP Semiconductors Germany GmbH, Business Unit Security and Connectivity located in Hamburg, Germany and they also act as the sponsor of the evaluation and certification. A Certification Report is intended to assist prospective consumers when judging the suitability of the IT security properties of the product for their particular requirements.

The Target of Evaluation – TOE (i.e., the Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1) consists of the Crypto Library V2.0 and the NXP Secure Smart Card Controller P61N1M3PVD/VD-1/VE-1. For ease of reading the TOE is often called “Crypto Library on SmartMX2”.

The evaluation of the TOE was conducted as a composite evaluation and uses the results of the CC evaluation of the underlying NXP Secure Smart Card Controller P61N1M3PVD/VE certified under the German CC Scheme on 18 June 2014 (*[HW CERT]*) and maintained to the P61N1M3PVD/VD-1/VE-1 on 16 October 2014 (*[HW MAINT]*).

The Crypto Library on SmartMX2 is a cryptographic library, which provides a set of cryptographic functions that can be used by the Smartcard Embedded Software. The cryptographic library consists of several binary packages that are intended to be linked to the Smartcard Embedded Software. The Smartcard Embedded Software developer links the binary packages that he needs to his Smartcard Embedded Software and the whole is subsequently implemented in the arbitrary memory. The NXP SmartMX2 smart card processor provides the computing platform and cryptographic support by means of co-processors for the Crypto Library on SmartMX2.

The Crypto Library on SmartMX2 provides The TOE provides AES, DES, Triple-DES (3DES), RSA, RSA key generation, RSA public key computation, ECDSA, ECC key generation, ECDH, ECC point addition, ECC curve parameter verification, SHA-1, SHA-224, SHA-256, SHA-384, SHA-512 algorithms, HMAC. In addition, the Crypto Library implements a software (pseudo) random number generator, which is initialised (seeded) by the hardware random number generator of the SmartMX2.

Finally, the TOE provides a secure copy routine and a secure compare routine and includes internal security measures for residual information protection. For more details refer to the *[ST]*, chapter 1.3.2.

The TOE has been evaluated by Brightsight B.V. located in Delft, The Netherlands. The evaluation was completed on 5 February 2015 with the final delivery of the ETR. The certification procedure has been conducted in accordance with the provisions of the Netherlands Scheme for Certification in the Area of IT Security *[NSCIB]*.

The scope of the evaluation is defined by the Security Target *[ST]*, which identifies assumptions made during the evaluation, the intended environment for the Crypto Library on SmartMX2, the security requirements, and the level of confidence (evaluation assurance level) at which the product is intended to satisfy the security requirements. Consumers of the Crypto Library on SmartMX2 are advised to verify that their own environment is consistent with the Security Target, and to give due consideration to the comments, observations and recommendations in this certification report.

The results documented in the evaluation technical report *[ETR]* for this product provide sufficient evidence that it meets the EAL6 augmented (EAL6+) assurance requirements for the evaluated security functionality. This assurance level is augmented with ALC_FLR.1 (Basic flaw remediation) and ASE_TSS.2 (TOE summary specification with architectural design summary).

The evaluation was conducted using the Common Methodology for Information Technology Security Evaluation, Version 3.1 Revision 4 *[CEM]*, for conformance to the Common Criteria for Information Technology Security Evaluation, version 3.1 Revision 4 *[CC]*.

TÜV Rheinland Nederland B.V., as the NSCIB Certification Body, declares that the Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1 evaluation meets all the conditions for international recognition of Common Criteria Certificates and that the product will be listed on the NSCIB Certified Products list. It should be noted that the certification results only apply to the specific version of the product as evaluated.

2 Certification Results

2.1 Identification of Target of Evaluation

The Target of Evaluation (TOE) for this evaluation is the Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1 from NXP Semiconductors Germany GmbH, Business Unit Security and Connectivity located in Hamburg, Germany.

This report pertains to the TOE which is comprised of the following main components:

Type	Name	Release	Date	Form of delivery
IC hardware	P61N1M3VD/VD-1	The IC hardware is base type P61N1M3VD and identified by its nameplate 9068B, which is located in the layout of the chip as described in [HW-UG-Wafer].		wafer with dice acc. to 9068B_BE_20130604.gds2.gz
	P61N1M3VE-1	The IC hardware is base type P61N1M3VE and identified by its nameplate 9068C, which is located in the layout of the chip as described in [HW-UG-Wafer].		wafer with dice acc. to 9068C_20130808.gds2.gz
IC Dedicated Test Software	Test-ROM Software	The IC Dedicated Software is identified by its NXP Content Number (NCN) set in Table 4 and 5 of [ST-HW-MAINT],which can be read out by the Security IC Embedded Software as described in [HW-P61-DATASHEET].		ROM code on the IC acc. to 9068B_DA005_TESTROM_v1_btos_0Ev13_fos_9v30rc4.hex (P61N1M3VD/VD-1) ROM code on the IC acc. to 9068C_DA007_TESTROM_v1_btos_0Ev15_fos_9v3.hex (P61N1M3VE-1)
IC Dedicated Support Software	Boot-ROM Software			
	Firmware Operating System			
	Bootloader Software			ROM code on the IC acc. to phBootloader_P61_Crc.hex
Library file	phSmx2ClAes.lib	1.1	2013-04-08	Electronic file
	phSmx2ClDes.lib	1.0	2013-01-30	Electronic file
	phSmx2ClRsa.lib	1.1	2013-08-02	Electronic file
	phSmx2ClRsaKg.lib	1.1	2013-10-29	Electronic file
	phSmx2ClEccGfp.lib	1.1	2013-10-29	Electronic file
	phSmx2ClSha.lib	1.0	2013-01-30	Electronic file
	phSmx2ClSha512.lib	1.0	2013-01-30	Electronic file
	phSmx2ClRng.lib	1.1	2013-04-08	Electronic file
	phSmx2ClUtils.lib	1.2	2013-07-30	Electronic file
	phSmx2ClSecSha.lib	1.0	2013-09-19	Electronic file
	phSmx2ClHmac.lib	1.0	2013-08-02	Electronic file
	phSmx2ClSymCfg.lib	1.0	2013-10-30	Electronic file
Header file	phSmx2ClAes.h	1.1	2013-04-08	Electronic file
	phSmx2ClDes.h	1.0	2013-01-30	Electronic file
	phSmx2ClRsa.h	1.1	2013-08-02	Electronic file
	phSmx2ClRsaKg.h	1.1	2013-10-29	Electronic file
	phSmx2ClEccGfp.h	1.1	2013-10-29	Electronic file
	phSmx2ClSha.h	1.0	2013-01-30	Electronic file
	phSmx2ClSha512.h	1.0	2013-01-30	Electronic file

Type	Name	Release	Date	Form of delivery
	phSmx2ClRng.h	1.1	2013-04-08	Electronic file
	phSmx2ClUtils.h	1.2	2013-07-30	Electronic file
	phSmx2ClUtils_ImportExportFcts.a51	1.2	2013-07-30	Electronic file
	phSmx2ClUtils_RngAccess.a51	1.2	2013-07-30	Electronic file
	phSmx2ClTypes.h	1.1	2013-11-15	Electronic file
	phSmx2ClSecSha.h	1.0	2013-07-19	Electronic file
	phSmx2ClHmac.h	1.0	2013-08-02	Electronic file
	phSmx2ClSymCfg.h	1.0	2013-10-30	Electronic file
Source code	phSmx2ClUtils_ImportExportFcts.a51	1.2	2013-07-30	Electronic file
	phSmx2ClUtils_RngAccess.a51	1.2	2013-07-30	Electronic file

To ensure secure usage a set of guidance documents is provided together with the Crypto Library on SmartMX2. Details can be found in section 2.5 of this report.

The hardware part of the TOE is delivered by NXP either as wafer, module, inlay, or packaged form together with the IC Dedicated Support Software. The Crypto Library is delivered in Phase 1 of the TOE lifecycle (for a detailed and precise description of the TOE lifecycle refer to the *[ST]*, chapter 1.2.2.) as a software package (a set of binary files) to the developers of the Smartcard Embedded Software. The Smartcard Embedded Software may comprise in this case an operating system and/or other smart card software (applications). The Software developers can incorporate the Crypto Library into their product.

As explained in the user guidance, as part of the delivery procedure, the customer shall verify the correctness of the delivered files by calculating the SHA-256 hash value of the delivered files and comparing them to reference values provided in the user guidance. For the identification of the Hardware please refer to section 2.8 of this report.

2.2 Security Policy

The TOE provides the cryptographic algorithms AES, DES, Triple-DES (3DES), RSA, RSA key generation, RSA public key computation, ECDSA, ECC key generation, ECDH, ECC point addition, ECC curve parameter verification, SHA-1, SHA-224, SHA-256, SHA-384, SHA-512 algorithms, and HMAC, in addition to the functionality described in the Hardware Security Target *[ST-HW-MAINT]* for the hardware platform. The cryptographic algorithms (except SHA) are resistant against Side Channel Attacks, including Simple Power Analysis (SPA), Differential Power Analysis (DPA), Differential Fault Analysis (DFA) and timing attacks. SHA is only resistant against Side Channel Attacks and timing attacks. Details on the resistance claims are provided in the Security Target *[ST],* relevant details are provided in the user guidance documents.

The TOE implements a software (pseudo) random number generator, which is initialised (seeded) by the hardware random number generator of the SmartMX2.

The TOE also a secure copy routine and a secure compare routine and includes internal security measures for residual information protection.

Note that the TOE does not restrict access to the functions provided by the hardware: these functions are still directly accessible to the Smartcard embedded Software.

2.3 Assumptions and Clarification of Scope

2.3.1 Assumptions

The Assumptions defined in the Security Target are not covered by the TOE itself. These aspects lead to specific Security Objectives to be fulfilled by the TOE-Environment. The following topics are of relevance:

- Usage of Hardware Platform,

- Ø Treatment of User Data,
- Ø Protection during Packaging, Finishing and Personalization,
- Ø Check of Initialisation Data by the Smartcard Embedded Software,

Details can be found in the Security Target *[ST]* chapter 4.

2.3.2 Clarification of scope

The evaluation did not reveal any threats to the TOE that are not countered by the evaluated security functions of the product.

2.4 Architectural Information

This chapter provides a high-level description of the IT product and its major components based on the evaluation evidence described in the Common Criteria assurance family entitled “TOE design (ADV_TDS)”. The intent of this chapter is to characterise the degree of architectural separation of the major components and to show dependencies between the TOE and products using the TOE in a composition (e.g. dependencies between HW and SW).

The TOE contains a Crypto Library, which provides a set of cryptographic functionalities that can be used by the Smartcard Embedded Software. The Crypto Library consists of several binary packages that are intended to be linked to the Smartcard Embedded Software. The Smartcard Embedded Software developer links the binary packages that he needs to his Smartcard Embedded Software and the whole is subsequently implemented in arbitrary memory. Please note that the crypto functions are supplied as a library rather than as a monolithic program, and hence a user of the library may include only those functions that are actually required. However, some dependencies exist; details are described in the User Guidance.

The TOE is implemented as a set of subsystems. The division into subsystems is chosen according to the cryptographic algorithms provided. The whole TOE provides AES, DES, Triple-DES (3DES), RSA, RSA key generation, RSA public key computation, ECDSA, ECC key generation, ECDH, ECC point addition, ECC curve parameter verification, SHA-1, SHA-224, SHA-256, SHA-384, SHA-512 and HMAC algorithms in addition to the functionality described in the Hardware Security Target *[ST-HW-MAINT]* for the hardware platform. In addition, the TOE implements a software (pseudo) random number generator, which is initialised (seeded) by the hardware random number generator of the SmartMX2.

The TOE also contains a secure copy routine and a secure compare routine and includes internal security measures for residual information protection.

2.5 Documentation

The following documentation is provided with the product by the developer to the customer:

Type	Name	Release	Date	Form of delivery
Document	SmartMX2 P61N1M3 Secure high-performance mobile secure controller, data sheet	3.1	2 September 2014	Electronic document
Document	P61N1M3 VD, NV Properties, data sheet addendum	1.0	22 November 2013	Electronic document
Document	P61N1M3 VE, NV Properties, data sheet addendum	1.0	22 November 2013	Electronic document
Document	Instruction Set for the SmartMX2 family, Secure smart card controller	3.1	2 February 2012	Electronic document
Document	Chip Health Mode (CHM) for P61N1M3, data sheet addendum	1.2	9 August 2013	Electronic document
Document	P61N1M3 Firmware interface specification, data sheet addendum	1.6	31 October 2013	Electronic document
Document	NXP Secure Smart Card Controller P61N1M3PVD/VD-1/VE-1 Information on Guidance and Operation	1.5	2 September 2014	Electronic document

Type	Name	Release	Date	Form of delivery
Document	SmartMX2 family P61N1M3 VD/VE Wafer and delivery specification, data sheet addendum	1.5	31 October 2013	Electronic document
Document	Trust Provisioning – Trust Provisioning concept and security architecture	1.8	19 May, 2014	Electronic document
Document	Key Delivery Procedures for Trust Provisioning	1.1	13 January 2014	Electronic document
Documents	User Guidance Manual	1.1	2014-11-17	Electronic document
	User Guidance: AES	1.0	2014-08-06	Electronic document
	User Guidance: DES	1.0	2014-08-11	Electronic document
	User Guidance: RSA	1.0	2014-08-08	Electronic document
	User Guidance: RSA Key Generation	1.0	2014-08-07	Electronic document
	User Guidance: ECC over GF(p)	1.0	2014-08-11	Electronic document
	User Guidance: SHA	1.0	2014-08-11	Electronic document
	User Guidance: SHA512	1.0	2014-08-07	Electronic document
	User Guidance: RNG	1.0	2014-08-11	Electronic document
	User Guidance: Utils	1.0	2014-08-11	Electronic document
	User Guidance: Secure SHA	1.0	2014-08-11	Electronic document
	User Guidance: HMAC	1.0	2014-08-11	Electronic document
	User Guidance: SymCfg	1.0	2014-08-11	Electronic document

2.6 IT Product Testing

Testing (depth, coverage, functional tests, independent testing): The evaluators examined the developer's testing activities documentation and verified that the developer has met their testing responsibilities.

2.6.1 Testing approach and depth

Testing by both the developer and evaluator was performed on the P61N1M3PVD, which was analysed by the evaluation lab and was concluded to be applicable to all hardware variations of the TOE.

The developer did extensive testing on FSP, subsystem and module level. All parameter choices have been addressed at least once. All boundary cases identified have been tested explicitly, and additionally the near-boundary conditions have been covered probabilistically. The testing was largely automated using industry standard and proprietary test suites. Test scripts were extensively used to verify that the functions return the expected values.

The hardware test results are extendable to composite evaluations on this hardware TOE, as the hardware is operated according to its guidance and the composite evaluation requirements are met.

For the testing performed by the evaluators, the developer has provided a testing environment. The evaluators have reproduced a selection of the developer tests, as well as a small number of test cases designed by the evaluator.

2.6.2 Independent Penetration Testing

The evaluator independent penetration tests were devised after performing an Evaluator Vulnerability Analysis. This was done in the following steps.

1. Inventory of required resistance
   This step used the JIL attack list *[JIL]* as a reference for completeness and studied the ST claims to decide which attacks in the JIL attack list applied for the TOE, as well as adding the evaluator's proprietary attack knowledge.
2. Validation of security functionalities
   This step identified the implemented security functionalities and performed evaluator

independent tests to verify implementation and to validate proper functioning of the security functions.

3. Vulnerability analysis
   In this step the design and the implementation of the security functionalities was studied and an analysis was performed to determine whether the implementation potentially could be vulnerable against the attacks of step 1. Based on this analysis the evaluators determined whether the design and implementation provide sufficient assurance or whether penetration testing is needed to provide sufficient assurance.
4. Penetration testing
   This step performed the penetration tests identified in step 4.
5. Conclusions on resistance
   This step performed a *[JIL]* compliant rating on the results of the penetration tests in relation with the assurance already gained by the design analysis. Based on the ratings the evaluators made conclusions on the resistance of the TOE against attackers possessing a high attack potential.
6. With the maintenance of the hardware, these steps were revisited and a gap analysis was made, leading to additional analysis and tests.

2.6.3 Test Configuration

Testing by both the developer and evaluator was performed on the P61N1M3PVD, which was analysed by the evaluation lab and was concluded to be applicable to all hardware variations of the TOE.

Since the TOE is not an end-user product it is not possible to perform testing without first embedding it in a testable configuration. To this end, the developer has created a proprietary test operating system. The main purpose of the test OS is to provide access to the crypto library's functionality. The test OS, and its documentation, was provided to the evaluators, and was used in all the testing. See the *[ETR]* for details.

2.6.4 Testing Results

The testing activities, including configurations, procedures, test cases, expected results and observed results are summarised in the *[ETR]*, with references to the documents containing the full details.

The developer's tests and the independent functional tests produced the expected results, giving assurance that the TOE behaves as specified in its ST and functional specification.

No exploitable vulnerabilities were found with the independent penetration tests.

2.7 Re-used evaluation results

No direct re-use has been made of previous evaluation results. Indirectly knowledge gained from evaluation of other similar TOEs has been used.

There has been extensive re-use of the ALC aspects for the sites involved in the software component of the TOE (NXP Semiconductors Hamburg, NXP Semiconductors Austria GmbH Styria, NXP Semiconductors Leuven). Sites involved in the development and production of the hardware platform were re-used by composition.

No sites have been visited as part of this evaluation.

2.8 Evaluated Configuration

The TOE is defined uniquely by its name and version number "Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1". The TOE consists of a hardware part and a software part. This certification covers the configurations of the TOE identified as follows:

The authenticity of the hardware part of the TOE is checked by visual inspection and by reading out the data stored in the memory.

- The die inscription on the surface of the TOE is verified to match the one documented in [HW-UG-Wafer].
- The data to be read includes the NXP Content Number NCN, the device coding byte DC(1), and the Fabkey number.

NXP Content Number (NCN) indicates the hardware base platform: 65 refers to the P61N1M3VD, 67 to the P61N1M3VD-1, 84 to the P61N1M3VE-1.

The FabKey number is not relevant for this evaluation. The Crypto Library does not make any use of FabKey data. This is data written into NV memory for personalization; it has no further influence on the Crypto Library.

The reference of the software part of the TOE is checked by calculating the SHA-256 hash value of the delivered files and comparing them to reference values provided in the user guidance.

2.9 Results of the Evaluation

The evaluation lab documented their evaluation results in the *[ETR]*[1] which references several Intermediate Reports and other evaluator documents. To support composite evaluations according to *[CCDB-2007-09-01]* a derived document *[ETRfC]* was provided and approved. This document provides details of the TOE evaluation that have to be considered when this TOE is used as platform in a composite evaluation.

The verdict of al claimed assurance requirements is: **Pass**

Based on the above evaluation results the evaluation lab concluded the Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1 to be **CC Part 2 extended, CC Part 3 conformant**, and to meet the requirements of **EAL6 augmented with ALC_FLR.1 and ASE_TSS.2**. This implies that the product satisfies the security technical requirements specified in Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1 Security Target, Revision 2.1, January 29, 2015.

The Security Target claims 'strict conformance' to the Protection Profile *[BSI-PP-0035]*.

2.10 Comments/Recommendations

The user guidance as outlined in section 2.5 contains necessary information about the usage of the TOE. Certain aspects of the TOE's security functionality, in particular the countermeasures against attacks, depend on accurate conformance to the user guidance of both the software and the hardware part of the TOE. There are no particular obligations or recommendations for the user apart from following the user guidance. Please note that the documents contain relevant details with respect to the resistance against certain attacks.
In addition all aspects of assumptions, threats and policies as outlined in the Security Target not covered by the TOE itself need to be fulfilled by the operational environment of the TOE.

The customer or user of the product shall consider the results of the certification within his system risk management process. In order for the evolution of attack methods and techniques to be covered, he should define the period of time until a re-assessment for the TOE is required and thus requested from the sponsor of the certificate.

The strength of the implemented cryptographic algorithms was not rated in the course of this evaluation. To fend off attackers with high attack potential appropriate cryptographic algorithms with adequate key lengths must be used (references can be found in national and international documents and standards).

The user of the Crypto Library must implement the advices of the hardware user guidance.

[1] The Evaluation Technical Report contains information proprietary to the developer and/or the evaluator, and is not releasable for public review.

Note that the certified TOE only includes the following three variants of the hardware platform: P61N1M3PVD, P61N1M3PVD-1, and P61N1M3PVE-1. This means that the Crypto Library 2.0 running on the P61N1M3PVE is not a certified configuration.

3 Security Target

The Security Target “Crypto Library V2.0 on P61N1M3PVD/VD-1/VE-1 Security Target, Revision 2.1, January 29, 2015” is included here by reference.

4 Definitions

This list of Acronyms and the glossary of terms contains elements that are not already defined by the CC or CEM:

BSI	Bundesamt für Sicherheit in der Informationstechnik
CBC	Cipher Block Chaining (a block cipher mode of operation)
CBC-MAC	Cipher Block Chaining Message Authentication Code
DES	Data Encryption Standard
DFA	Differential Fault Analysis
ECB	Electronic Code Book (a block cipher mode of operation)
IC	Integrated Circuit
IT	Information Technology
ITSEF	IT Security Evaluation Facility
NSCIB	Nederlands Schema voor Certificatie op het gebied van IT-Beveiliging
PP	Protection Profile
PRNG	Pseudo Random Number Generator
RMI	Remote Method Invocation
RSA	Rivest-Shamir-Adleman Algorithm
SHA	Secure Hash Algorithm
SPA/DPA	Simple/Differential Power Analysis
TOE	Target of Evaluation

5 Bibliography

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